# FINAL REPORT

## for

# NIMBUS Tracking and Data Relay Experiment Receivers

(2 January 1973 - 10 December 1974)

Contract No.: NAS-5-21902

Goddard Space Flight Center

Contracting Officer: John E. Firmin
Technical Monitor: John K. Steckel


Prepared by:

American Electronic Laboratories
Colmar, Pennsylvania

Project Manager: James Van Cleave


for

National Aeronuatics and Space Administration
Goddard Space Flight Center
Greenbelt, Maryland

Typed by

Proofed by

FINAL REPORT

for

# NIMBUS TRACKING AND DATA RELAY EXPERIMENT RECEIVERS

(2 January 1973 - 10 December 1974)

Contract No. NAS-5-21902

Prepared by
American Electronic Laboratories, Inc.
Colmar, Pennsylvania

for

National Aeronautics and Space Administration
Goddard Space Flight Center
Greenbelt, Maryland

Typed by ____________

Proofed by ____________

## ABSTRACT

This report summarizes the contracted effort for the production of improved design of Tracking and Data Relay Experiment (T&DRE) Receivers accomplished under NASA GSFC contract NAS-5-21902. Only these areas that were significantly changed over the previous design accomplished under contract NAS-5-10771 are discussed herein. Thus this report should be considered as an addendum to the October 1972 AEL report entitled "Tracking and Data Relay Experiment Receiver".



Typed by ____________

Proofed by ____________

## TABLE OF CONTENTS



## LIST OF APPENDICES



## LIST OF ILLUSTRATIONS





Typed by

Proofed by

## LIST OF ILLUSTRATIONS (cont)





Typed by ____________

Proofed by ____________

## Section 1

## Description of Receiver Design Changes

### 1.1 GENERAL

Figure 1 shows the NIMBUS T&DRE Receiver block diagram, as produced under this contract (NAS-5-21902). The reader is referred to Figure 4 of the final report for the previous effort, contract NAS-5-10771, for comparison purposes. The changes associated with each module are described in this section. A photograph of the complete receiver is shown in Figure 2.

The RF amplifier substrate and RF filter mixer substrate are contained in the lower tray, as the previous design. The middle tray now contains 1) the 40 MHz IF printed wiring board and second mixer and 2) the 2.4 MHz IF wiring board, including line filters. The 2.4 MHz interconnection between middle and top trays is now established at a 50-ohm termination for lowest VSWR and EMI due to ground currents. The upper tray is similar to that previously supplied and contains 1) 2.4 MHz line driver (now with added buffering) 2) signal strength circuit 3) narrowband discriminator and 4) command data amplifier, the latter three substrates similiar to that previously supplied.

Refer to Appendix I for a test report on the T&DRE Receiver. Appendix II gives parts listing by module and Appendix III presents acceptance test procedure and test results for S/N 2A, 3A, 4A.

### 1.2 RF MODULE

#### 1.2.1 2062 MHz RF Amplifier

The 2062 MHz RF amplifier was comprised of a two-stage common emitter amplifier using the HP 35822 transistor. Both stages are now constructed on a common alumina substrate approximately 0.75 inch x 1.5 inch using thin-film techniques and aligned for maximum performance. This design combines the previous two substrates into a single substrate for improved integrity. Each amplifier stage is tuned by changing the length of quarter-wave stubs on the base and collector circuits.

The two-stage RF amplifier has a total gain at the 2062 MHz center frequency of 18 dB at a nominal 12 volt DC supply input at 4 milliamps drain. The input VSWR is less than 1.5:1 at the input connector to the RF amplifier and the noise figure is typically 5 dB. The HP 35866 device supersedes use of the discontinued Avantek AT-101 device, and possesses a lower noise figure (3.0 dB) plus higher available gain (11.5 dB) at 2 GHz. Minor impedance matching modification was performed.



Typed by ____

Proofed by ____

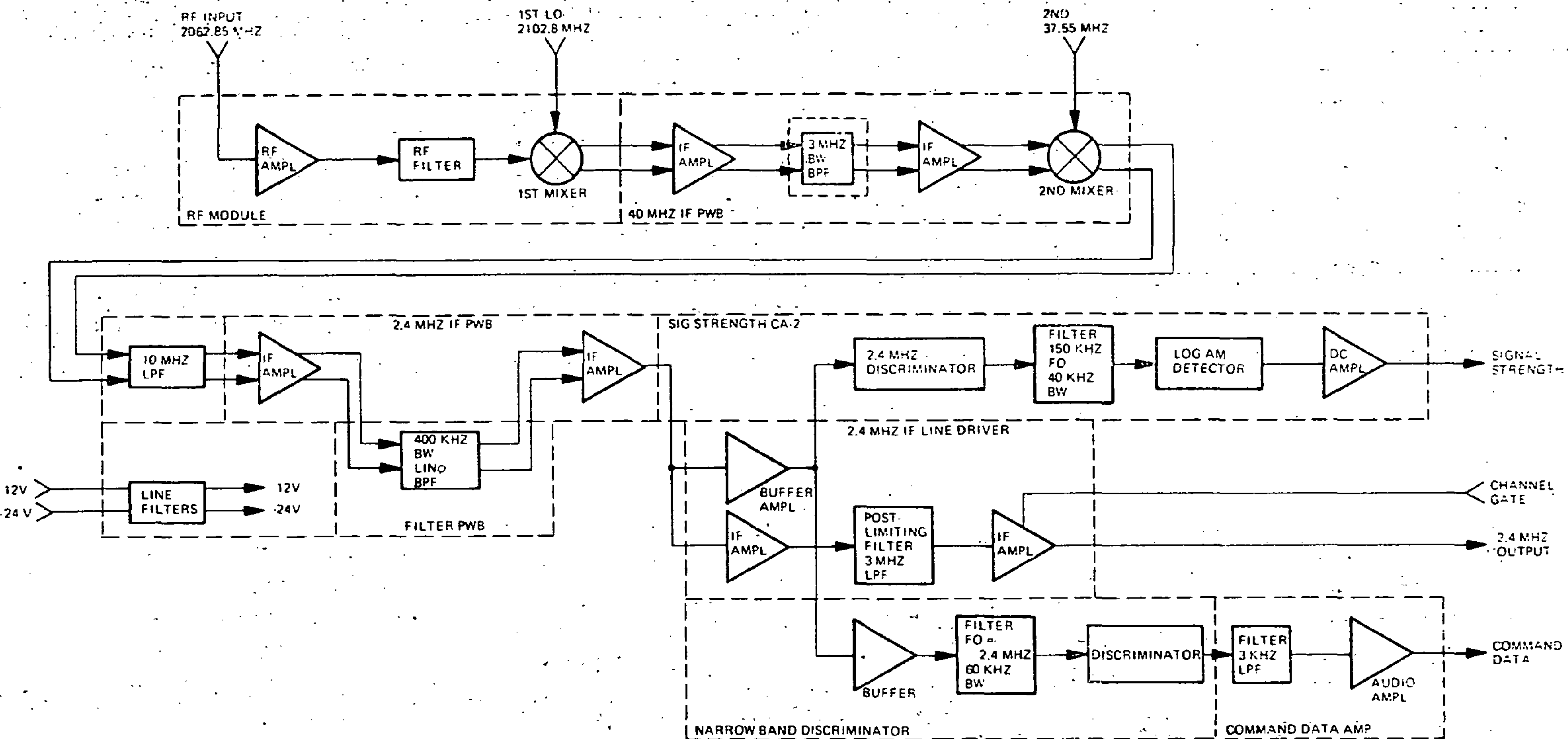



Figure 1. NIMBUS T&DRE Receiver, Block Diagram



Typed by

Proofed by

Figure 2. T&DRE Receiver, External View.



Typed by

Proofed by

Fig 3

The RF module schematic did not change from that previously, except that the RF transistors in the RF amplifier were changed to a HP35866E type and the thick-film resistor values were modified slightly. Figure 3 shows the new RF amplifier circuitry of the RF module.

Upon interface with the diplexer, it was determined that the RF amplifier could oscillate at some out-of-band frequency. It was determined that a 3 dB pad at the receiver RF input eliminated this difficulty at the expense of sensitivity.

### 1.2.2 RF Filter and First Mixer

Fig 4

The RF filter and first mixer circuitry, shown in Figure 4, did not change from the previous design. The RF filter is composed of two basic filter types, the first being a three element short stub band reject filter with a maximum insertion loss of 30 dB placed at a frequency of 2143 MHz and the second filter, a three section parallel coupled bandpass filter with a center frequency of 2063 MHz. Each of these filters and the single-balanced mixer are assembled on one common substrate approximately 4.5 inches long by 1.5 inches wide using thin film techniques. The nominal loss at the center frequency of 2063 MHz through the two filters and the mixer is 10 dB giving the overall RF amplifier, with conversion loss, a total gain of 8 dB. The nominal rejection of the two filters to the primary image frequency of 2143 MHz is 56 dB, and this rejection coupled with the approximate 4 dB loss through the RF amplifier at the image frequency combine to give a total design center value image rejection of 60 dB. The first mixer is a single-balanced type requiring a LO drive of 3 milliwatts at a nominal frequency of 2102 MHz. The overall conversion loss of the first mixer is 5 to 6 dB.

## 1.3 <u>40 MHz IF AMPLIFIER AND SECOND MIXER</u>

Fig 5 Fig 6

The 40 MHz IF circuitry and construction significantly changed due to 1) use of balanced rather than single ended coupling 2) use of a printed wiring board rather than HIC substrate construction and 3) placement of the bandpass filter on a separate board below the 40 MHz IF amplifier board. The 40 MHz IF is contained within the middle tray, as shown in Figure 5. The schematic of the 40 MHz amplifier is shown in Figure 6.

Fig 7 Fig 8

The modified 40 MHz amplifier is fabricated using printed circuit construction on copper-clad G-10 material with discrete RCR resistors and CYK Corning capacitors. This new board has the same physical dimensions as the former thick-film units and occupies the same position in the middle tray. Figure 7 and 8 shows the 40 MHz IF amplifier board, top and bottom, respectively.

Fig 9

Figure 9 shows the assembly drawing of the 40 MHz amplifier bond. board



Typed by ______

Proofed by ______

Figure 3. RF Amplifier.



Typed by ____________

Proofed by ____________

Figure 4. RF Filter and Mixer.



Typed by ______________

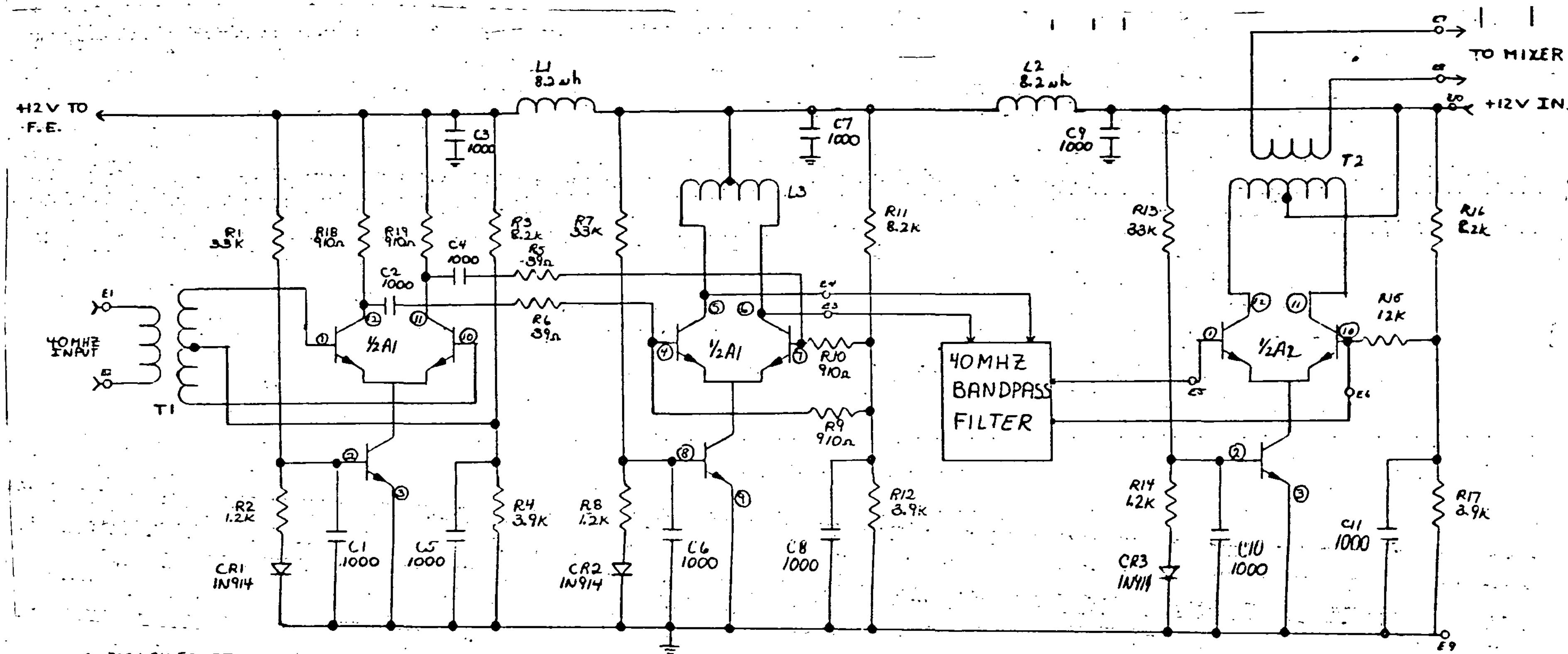
Proofed by ______________

Figure 5. Receiver Middle Tray.



Typed by ____________

Proofed by ____________




ALL CAPACITOR VALUES ARE IN PF

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY MIL-D-1000.
DO NOT SCALE DRAWING.
UNLESS OTHERWISE SPECIFIED.
DIMENSIONS ARE IN INCHES AND INCLUDE PLATING THICKNESS WHEN SPECIFIED.
ALL THREADS ARE UNIFIED NATIONAL SERIES, CLASS 2.
REMOVE ALL BURRS AND SHARP EDGES.
MANUFACTURE IN ACCORDANCE WITH MFG SPEC NO.
* VENDOR ITEM-SEE SPECIFICATION OR SOURCE CONTROL DRAWING.
† VENDORS IDENTIFIED BY CODE IDENT NO. ARE LISTED IN FEDERAL CATALOGING HANDBOOK H4-2.

Figure 6. 40 MHz IF Amplifier Schematic.

Figure 7. 40 MHz Amplifier, Top View.

Figure 8. 40 MHz Amplifier, Bottom View.

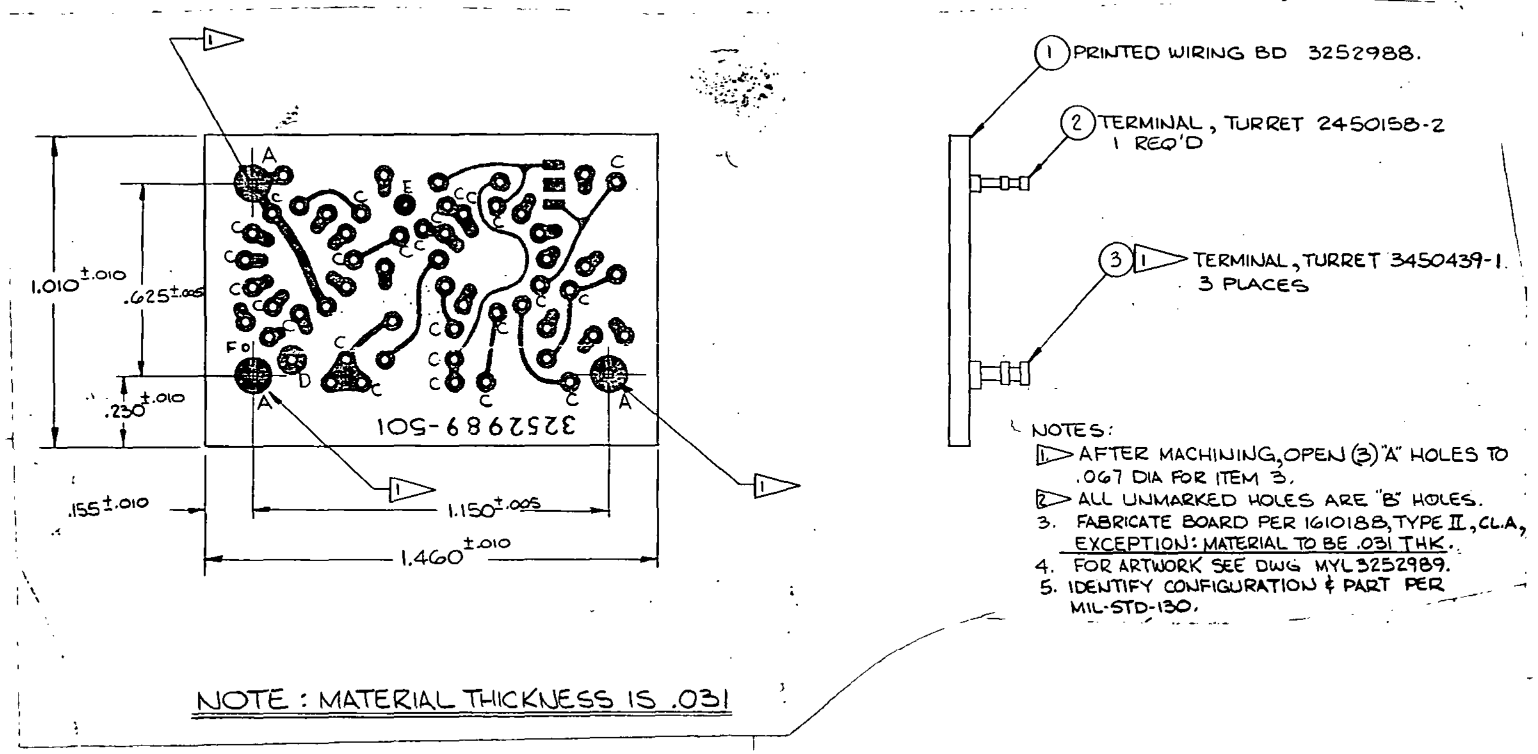



Figure 9. 40 MHz Amplifier Assembly.



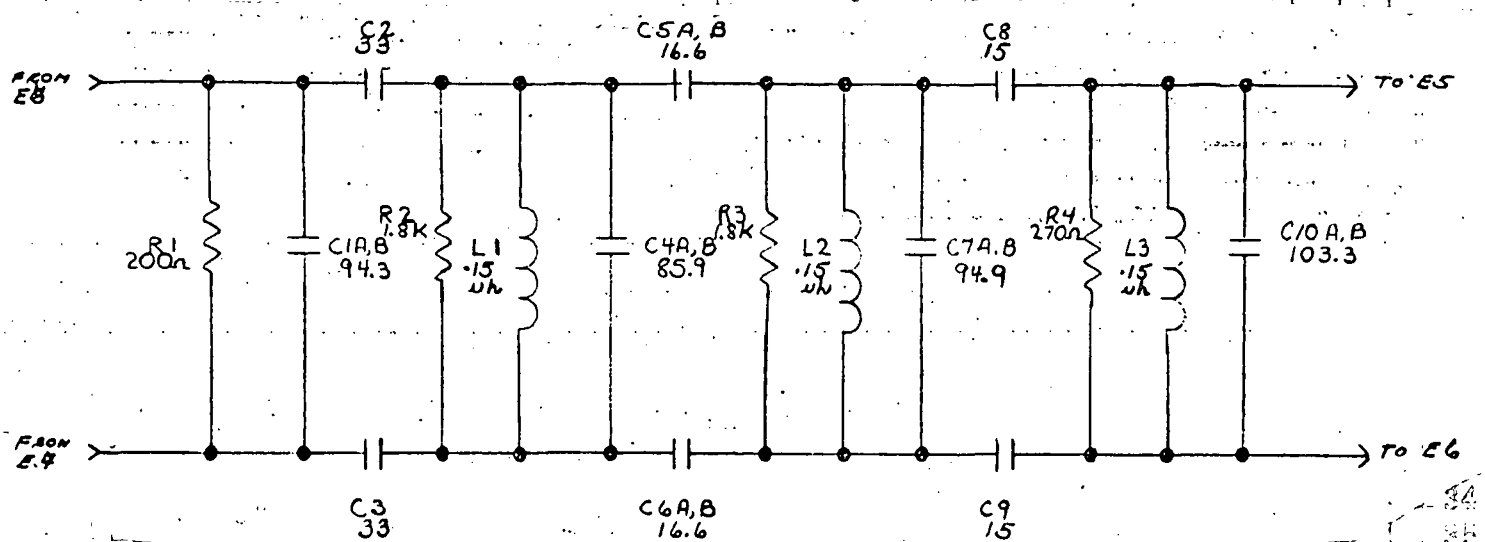
Typed by __________

Proofed by __________

The input signal is initially balanced with respect to ground at transformer T1 and remains so balanced throughout the middle tray taking advantage of the common mode rejection properties of the RCA CA-3049 dual differential amplifier IC's. Amplifiers A1 and A2 have a collective gain of 30 dB with A2 driving a 250 ohm balanced input four-section linear phase bandpass filter. This filter is shown schematically in Figure 10 and has a nominal 3 dB bandwidth of 4 MHz centered at 39.95 MHz with a loss of 8 dB. Figure 11 shows a photograph of the 40 MHz IF filter board and figure 12 shows the assembly. The 40 MHz IF filter is fabricated using thick film techniques and uses screened on resistors and chip capacitors. This new filter board is placed in a well beneath the 40 MHz amplifier. Fig 12

Amplifier A3 adds an additional 16 dB of gain and drives a double balanced mixer through the step-down transformer T2.

The second mixer in an HP 10534C double balanced unit with all outputs isolated. The isolation of all outputs allows for a completely balanced signal design and eliminates ground coupling between the 40 MHz signal, the 37.55 MHz LO, and the 2.4 MHz amplifiers.




ALL CAPACITOR VALUES ARE IN PF

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY MIL-STD-100
DO NOT SCALE DRAWING.
UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES AND INCLUDE PLATING THICKNESS WHEN SPECIFIED.
ALL THREADS ARE UNIFIED NATIONAL SERIES, CLASS 2.
REMOVE ALL BURRS AND SHARP EDGES.
MANUFACTURE IN ACCORDANCE WITH MFG SPEC NO. 161005.
* VENDOR ITEM-SEE SPECIFICATION OR SOURCE CONTROL DRAWING.
+ VENDORS IDENTIFIED BY CODE IDENT NO. ARE LISTED IN FEDERAL CATALOGING HANDBOOK H4-2.

Figure 10. 40 MHz Bandpass Filter Schematic.



Typed by ____________

Proofed by ____________

Figure 11. 40 MHz Bandpass Filter.

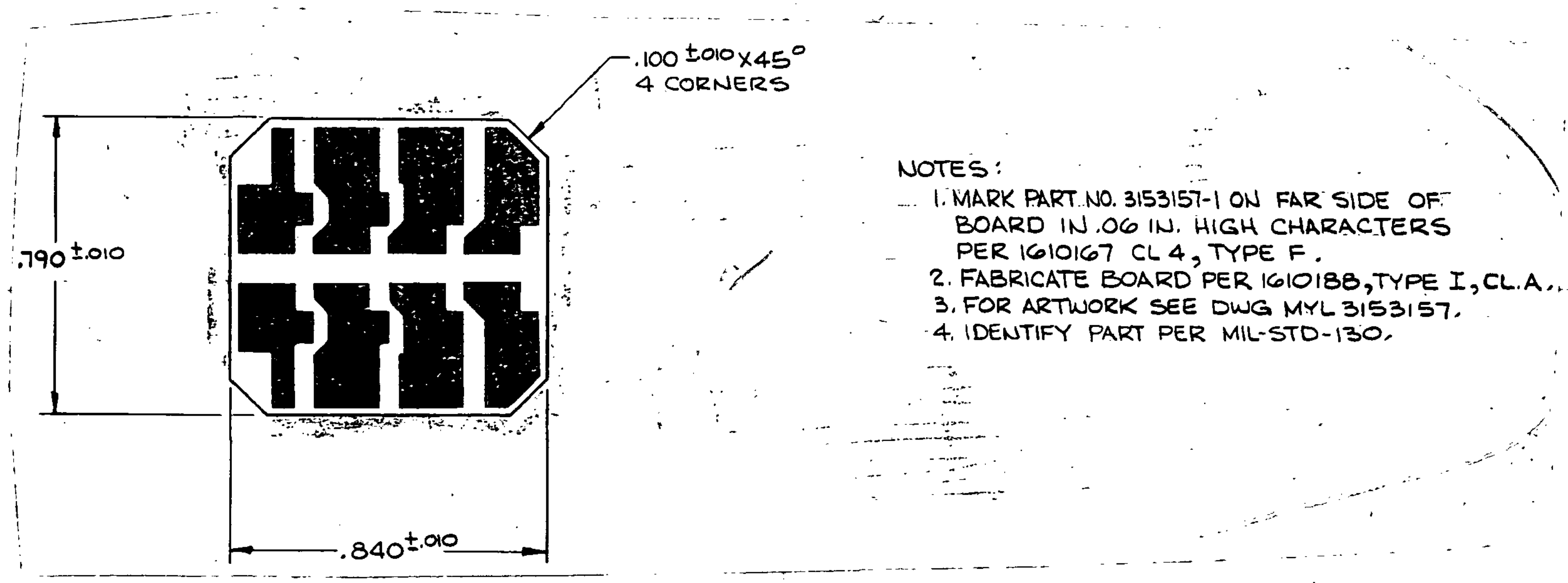



Figure 12. 40 MHz Bandpass Filter Assembly.

## 1.4 2.4 MHZ AMPLIFIER AND CHANNEL FILTER

The new 2.4 MHz amplifier is of printed-circuit construction on copperclad G-10 material using discrete RCR resistors and CYK Corning capacitors and occupies the area formerly used by the CA-1A substrate and the line filter substrate.

The power line filters are included on the 2.4 MHz IF amplifier board, and attenuate EMI on the +12 V and -24.2 V power lines.

Figure 13 is the schematic of the 2.4 MHz IF amplifier. A balanced signal approach is used to eliminate ground loops and to take advantage of the common mode rejection of the CA-3049. The balanced input from the second mixer is passed through a balanced 10 MHz low pass filter made up of L1, L2, L9 and L10 with C1 and C22 to eliminate LO feedthrough components from the 2.4 MHz signal. Amplifiers A1 and A2 produce a cummulative gain of 46 dB and provide a balanced drive to the 2.4 MHz bandpass filter. Figure 14 is a photograph of the 2.4 MHz IF amplifier top, Figure 15 is the bottom side, and Figure 16 is the assembly drawing.

Figure 17 is the 2.4 MHz bandpass filter schematic diagram. The design is a balanced five-section linear phase (equiripple) design with all components fixed tuned. The nominal 3 dB bandwidth is 400 kHz with an equivalent noise bandwidth of 520 kHz.

The 2.4 MHz channel filter is of thick-film construction using screened on resistors and chip capacitors and is placed in the well beneath the new 2.4 MHz amplifier board. Figure 18 is a photograph of the early 2.4 MHz bandpass filter and Figure 19 is the assembly drawing. A later technique is described in section 2.4 of this report.

Referring back to Figure 13, the last two differential amplifier gain stages are operated at 10 V as fixed by VR1 through R17. Since amplifier A4 is always in limiting, a constant peak-to-peak output for supply voltage variations is maintained. Transformer T1 drives the 50-ohm interconnecting cable external to the receiver which connects the 2.4 MHz IF amplifier to the line driver board.

## 1.5 LINE DRIVER BOARD

The line driver board is modified and will be fabricated with printed-circuit construction, RCR and CYK discrete components, and JAN TX 2N918 transistors. Figure 20 is the schematic diagram for the line driver board. This line driver schematic is identical with the previous units with the addition of Q1 which will further buffer the signal strength board and the narrowband command data board from the 2.4 MHz IF signal. Photographs of the top and bottom of the line driver board is shown in Figure 21 and 22 respectively. Figure 23 is the assembly drawing.

## 1.6 2.4 MHZ SIGNAL STRENGTH (Channel Amp #2)

The signal strength circuitry is virtually unchanged, except for layout modifications. The 2.4 MHz signal strength circuitry contains a wideband FM discriminator, a bandpass



Typed by ______

Proofed by ______

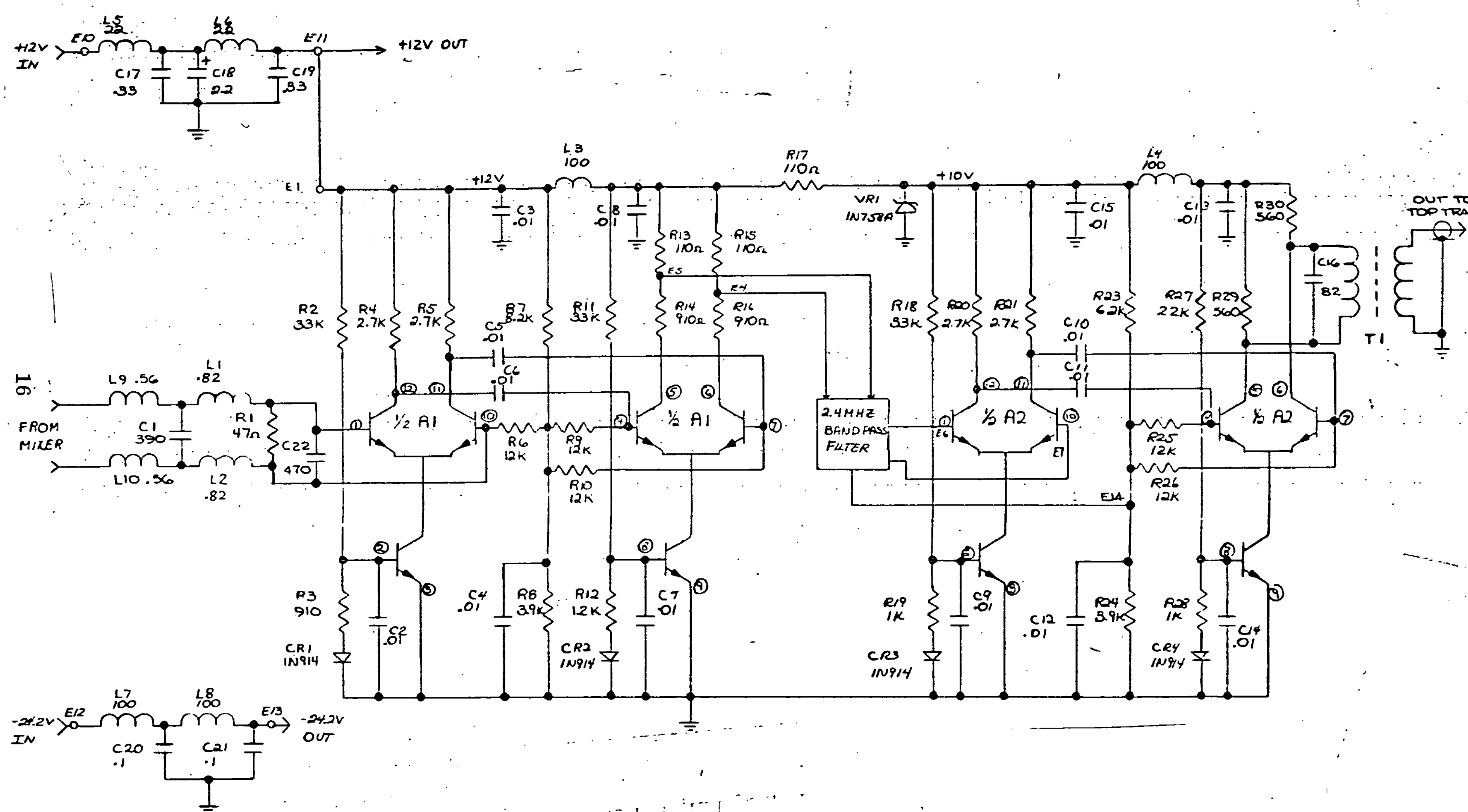



Figure 13. 2.4 MHz IF Amplifier Schematic.



Typed by ____________

Proofed by ____________

Figure 14. 2.4 MHz IF Amplifier, Top View.



Typed by ________________

Proofed by ________________

Figure 15. 2.4 MHz IF Amplifier, Bottom View.



Typed by ____________________

Proofed by ____________________

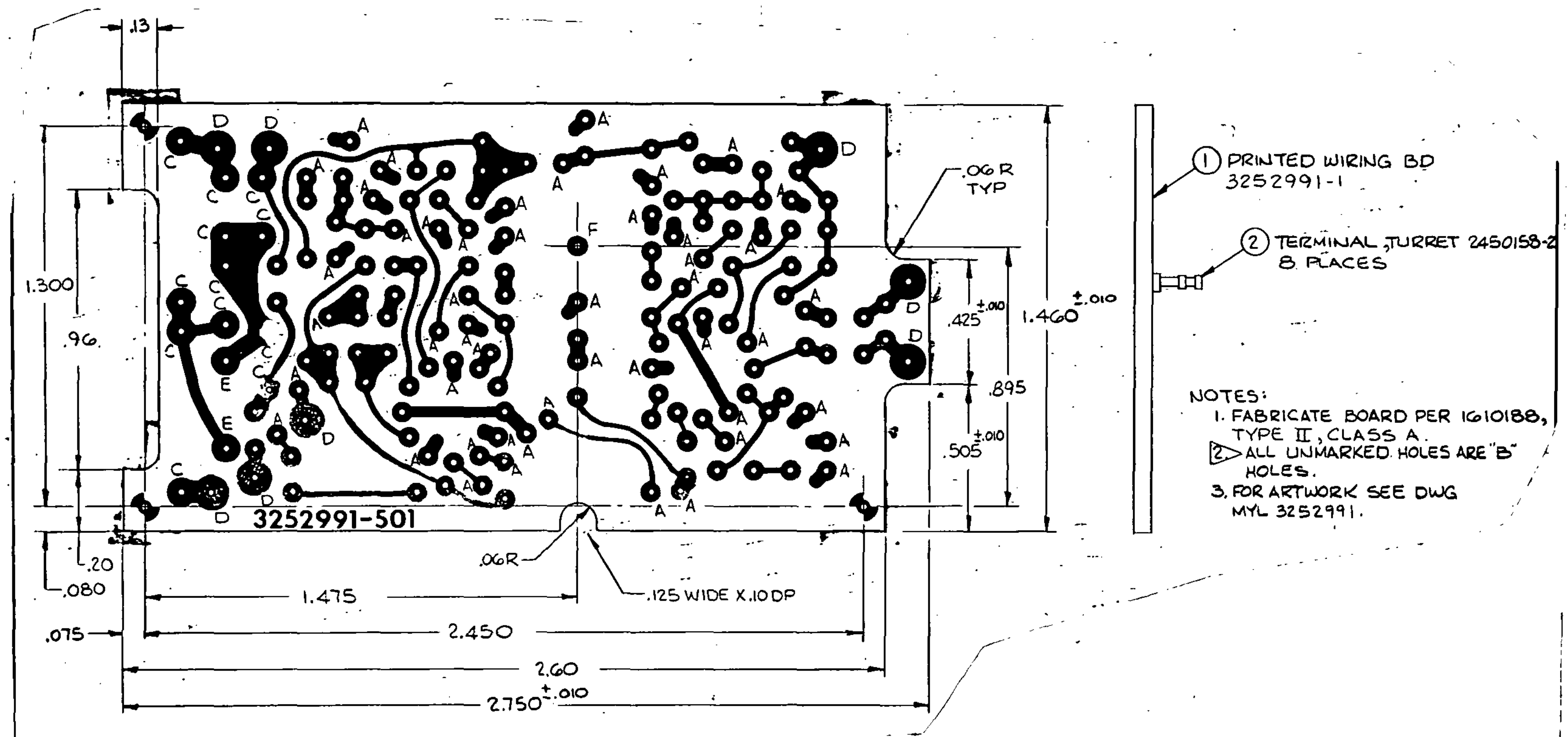
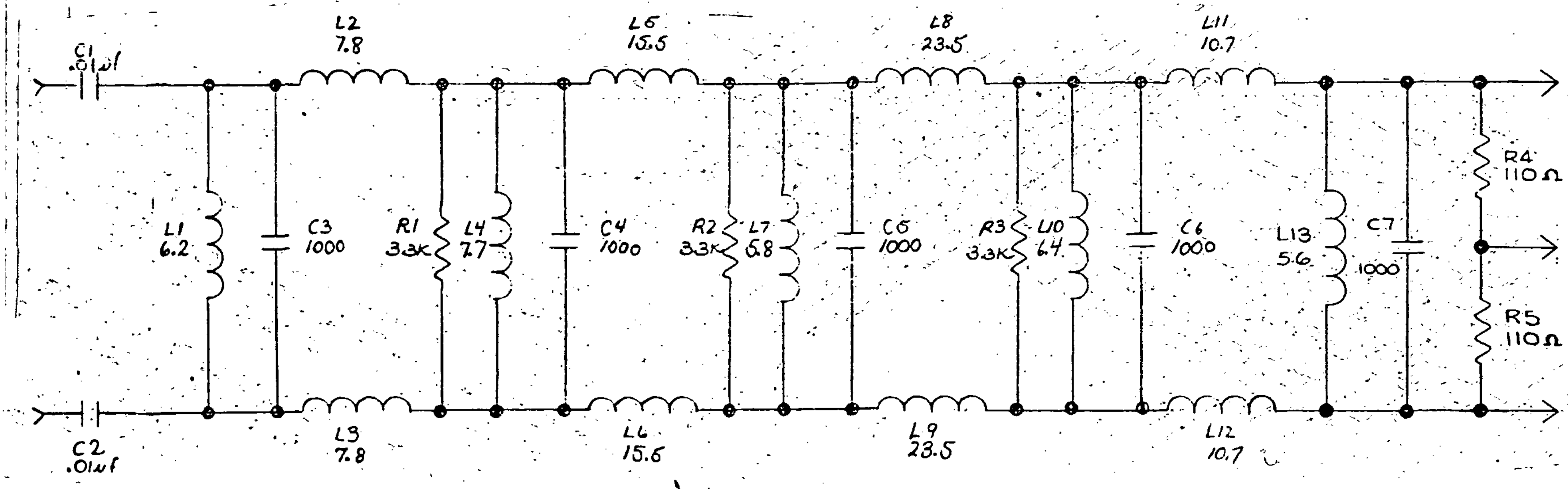



Figure 16. 2.4 MHz IF Amplifier Assembly.



Typed by

Proofed by




INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY MIL-STD-100
DO NOT SCALE DRAWING.
UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES AND INCLUDE PLATING THICKNESS WHEN SPECIFIED.
ALL THREADS ARE UNIFIED NATIONAL SERIES, CLASS 2.
REMOVE ALL BURRS AND SHARP EDGES.
MANUFACTURE IN ACCORDANCE WITH MFG SPEC NO. 161005.
* VENDOR ITEM-SEE SPECIFICATION OR SOURCE CONTROL DRAWING.
+ VENDORS IDENTIFIED BY CODE IDENT NO. ARE LISTED IN FEDERAL CATALOGING HANDBOOK H4-2.

Figure 17. 2.4 MHz Bandpass Filter Schematic.

Figure 18. 2.4 MHz Bandpass Filter.



Typed by ____________

Proofed by ____________

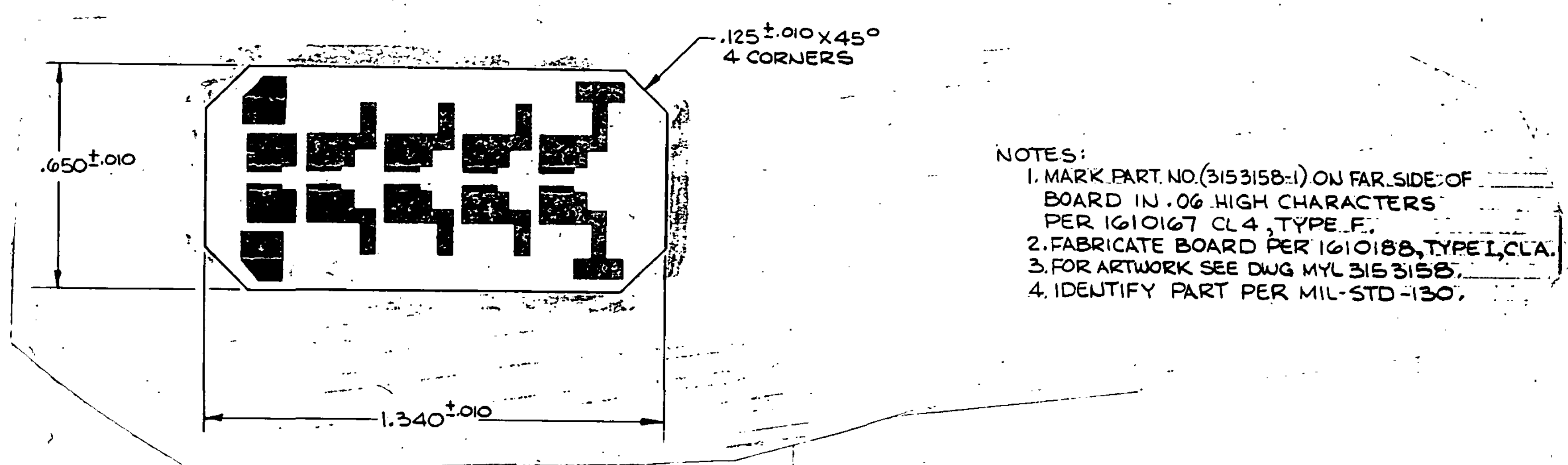



Figure 19. 2.4 MHz Bandpass Filter Assembly.



Typed by

Proofed by

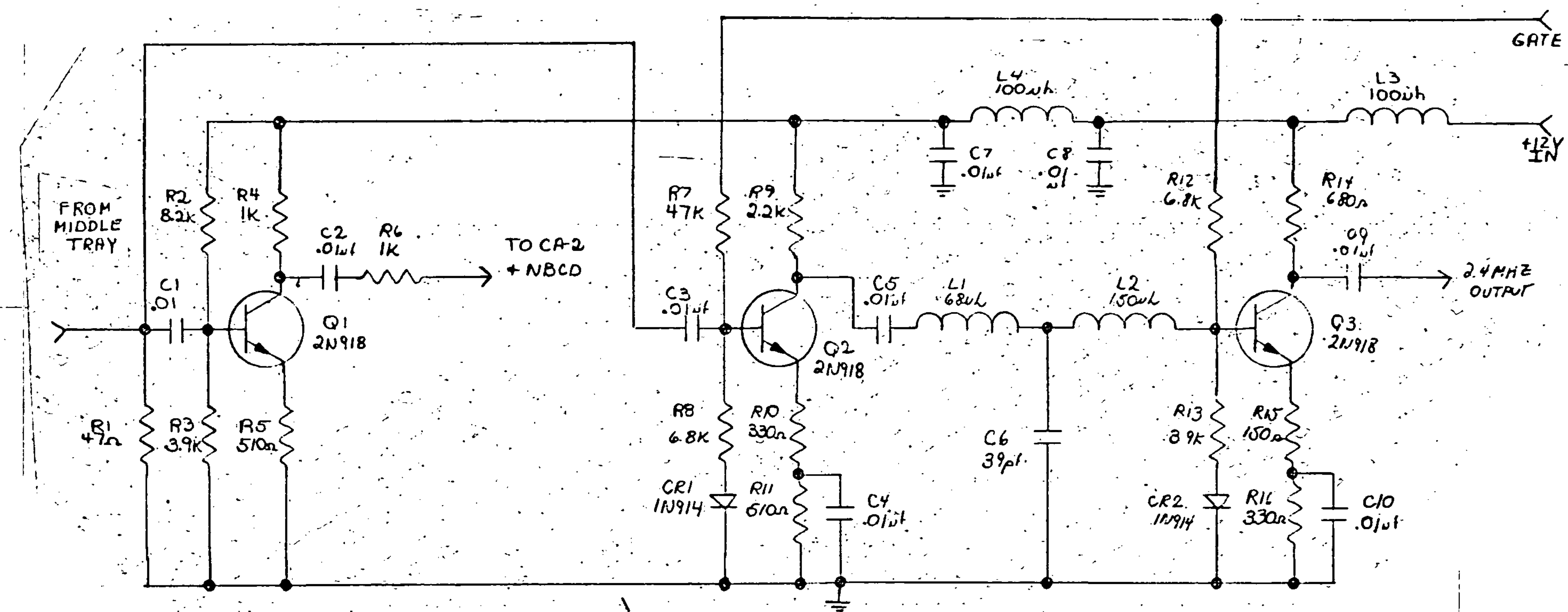



Figure 20. Line Driver Schematic.



Typed by ______

Proofed by ______

Figure 21. Line Driver, Top View.



Typed by ______________

Proofed by ______________

Figure 22. Line Driver, Bottom View.



Typed by ______________

Proofed by ______________

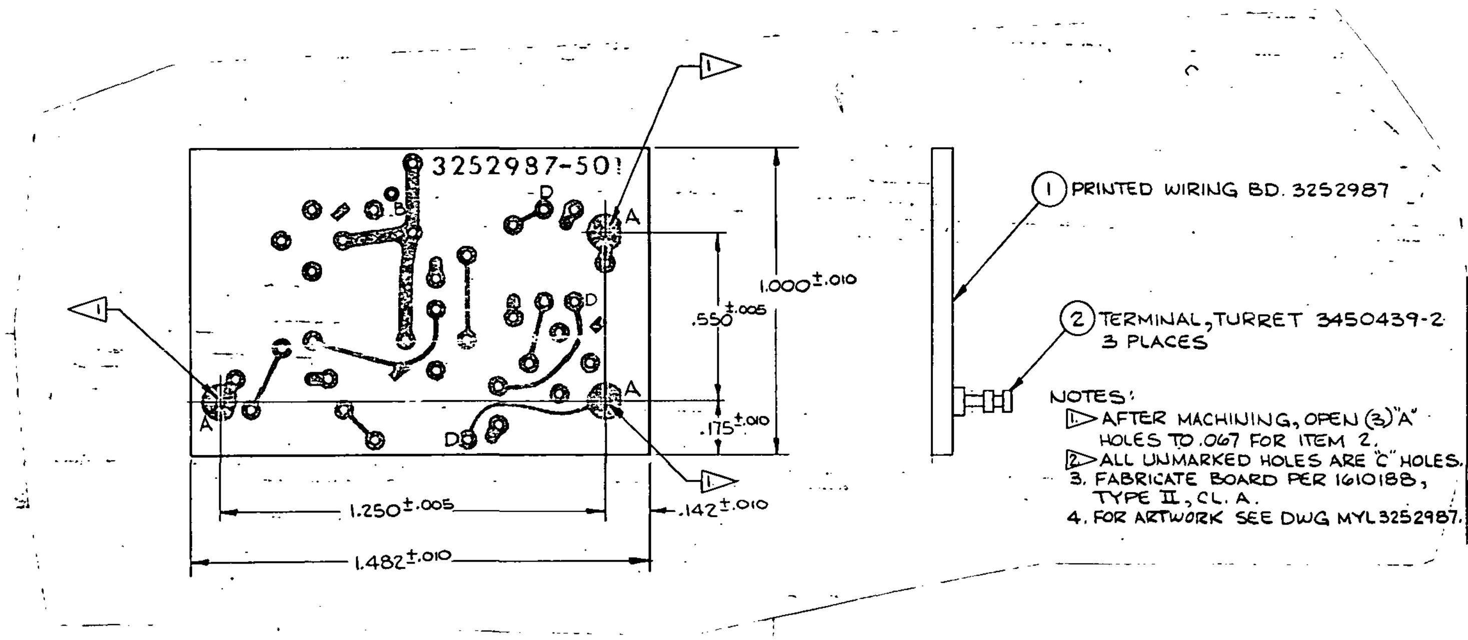



Figure 23. Line Driver Assembly.



Typed by ____________

Proofed by ____________

filter centered at 150 kHz, and a logarithmic AM detector. The signal strength schematic is shown in Figure 24, the substrate top view is shown in Figure 25 and bottom view in Figure 26. Figure 27 and 28 shows the assembly drawings.

## 1.7 NARROWBAND COMMAND DATA DETECTOR

The narrowband command data detector schematic is as shown in Figure 29, and is composed of an amplifier, a narrowband filter, limiter, and an emitter coupled quadrature detector located on one substrate (Figure 30 and 31) and an amplifier section called command data amplifier per schematic shown in Figure 32 which is located on a separate substrate.

The command data amplifier photograph is shown in Figure 33, and assembly drawing in Figure 34. Both the narrowband command data detector and amplifier circuits are nearly identical (minor layout changes) to that previously produced. The narrowband command data, signal strength, and line driver modules are housed in the top tray, per Figure 35.

Fig 24, 25, 26, 27, 28

Fig 29, 31, 30, 33, 32, 34, 35



Typed by .

Proofed by. cm